CLAIMS

What is claimed is:

1. An electrostatic discharge (ESD) protection device having a first terminal and a second terminal, the device comprising:

a transistor having a collector coupled to the first terminal of the ESD protection circuit, a base and an emitter coupled to the second terminal of the ESD protection circuit; and

a zener diode having a first terminal coupled to said collector of said transistor and a second terminal coupled said base of said vertical transistor wherein said zener diode breaks down in an ESD event providing impact ionization current to a base region of said transistor and wherein subsurface current paths are provided in said base region to redistribute current away from a surface of said base region to increase a peak current handled by the ESD protection device.

2. The device as recited in claim 1 further including:

a substrate of a first type;

an epitaxial layer of a second type; and

an isolation region formed in said epitaxial layer for defining an active area of the ESD protection device, said active area corresponding to said epitaxial layer interior to said isolation region.

3. The device as recited in claim 2 wherein said isolation region is of said first type.

4. The device as recited in claim 3 wherein said isolation region comprises a deep trench.

5. The device as recited in claim 2 further including:

a base region of said first type formed in said active area;

an emitter region of said second type formed in said base region, said emitter region coupling to the second terminal of the ESD protection device;

a first region of said first type formed in said base region, said first region being spaced a predetermined distance from said emitter region; and

a second region of said first type formed in said first region, said second region coupling to the second terminal of the ESD protection device wherein a depth of said first region into said base region is greater than a depth of said second region.

6. The device as recited in claim 5 wherein said doping concentration of said second region is greater than a doping concentration of said first region.

7. The device as recited in claim 6 wherein said first region is formed in a ring shape and wherein said emitter region is centrally located interior to said ring shape of said first region and wherein a depth of said first region in said base region is greater than a depth of said emitter region.

8. The device as recited in claim 7 further including:

a buried layer of said second type underlying a portion of said active area; and

a third region of said second type spaced a predetermined distance from said base region, said third region coupling to said buried layer and the first terminal of the ESD protection device.

9. The device as recited in claim 8 wherein said third region is formed in a ring shape and wherein said base region is located interior to said ring shape of said third region.

10. The device as recited in claim 9 further including a fourth region of said first type formed overlying a boundary between said base region and said epitaxial layer.

11. The device as recited in claim 10 wherein said zener diode comprises said fourth region, said epitaxial layer, and said third region.

12. A method of protecting a semiconductor device from an electrostatic discharge comprising the steps of:

breaking down a zener diode during an electrostatic discharge (ESD) event such that an impact ionization current is generated; and

enabling a transistor with said impact ionization current to dissipate said ESD event before the semiconductor device is damaged wherein said impact ionization current is distributed uniformly through a base region of said transistor to prevent current crowding at a surface of said base region.

13. The method as recited in claim 12 further including a step of distributing said ionization current below a surface of said transistor.

14. The method as recited in claim 12 further including a step of reducing a resistance in a path of said impact ionization current.

15. An electrostatic discharge (ESD) device having a first terminal and a second terminal, the ESD device comprising:

a substrate of a first type;

an epitaxial layer of a second type overlying said substrate;

an isolation region formed in said epitaxial layer to define an active area of the ESD device;

a base region of said first type formed in said epitaxial layer interior to said isolation region;

an emitter region of said second type formed in said base region, said emitter region coupled to the second terminal;

a first region of said first type formed in said base region adjacent to said emitter region wherein said first region has a depth greater than 30% of a depth of said base region and wherein said first region is coupled to said emitter region; and

a zener diode having a first terminal coupled to said epitaxial layer interior to said isolation region and a second terminal coupled to said base region.

16. The ESD device as recited in claim 15 further including a second region of said first type formed in said first region of said first type wherein said first region has a higher doping concentration than said base region and wherein said second region has a higher doping concentration than said first region.

17. The ESD device as recited in claim 16 further including:

a buried layer underlying said base region;

a third region of said second type formed in said epitaxial layer interior to said isolation region, said third region extending from a surface of said epitaxial layer to said buried layer; and

a fourth region of said second type formed in said third region, said fourth region coupling to the first terminal of the ESD device.

18. The ESD device as recited in claim 17 further including a fifth region of said first type overlying a boundary of between said base region and said epitaxial region interior to said isolation region.

19. The ESD device as recited in claim 18 wherein said fifth region and said third region are spaced a predetermined distance apart and wherein said zener diode comprises said third region, said epitaxial region interior to said isolation region, and said fifth region.

20. The ESD device as recited in claim 19 wherein the first terminal of the ESD device couples to circuitry of an integrated circuit to be protected and wherein said the second terminal of the ESD device couples to ground.